# 「多位元邏輯閘控制軟體之軟體建置及服務」規格需求 Boulder Opal and Scale Up Software Automation

#### Part 1: Delivery: Dec. 16, 2024

#### **Onsite Software Installation:**

 Q-CTRL R&D team will conduct onsite installation of software at the Academia Sinica Lab.

## • Two-qubit gate and GHZ demonstration

Deliverable 1: Experiment initialization and technical handoff

**Description:** Set up the prerequisite infrastructure and information handoff to complete the POC. This includes a technical briefing between Sinica and Q-CTRL to understand the current hardware states and formalize the official Target Values and setting up the necessary network access to Sinica HW.

**Success Criteria:** Q-CTRL confirms all baseline metrics have been gathered, final target values set, and stable device access has been achieved.

Deliverable 2: Experimentally tested two-qubit gate protocols.

**Description:** Q-CTRL will create a process to design, calibrate, and optimize a twoqubit gate waveform with the goal to maximize gate fidelity on current 5-qubit devices. **Success Criteria:** Q-CTRL demonstrates performance at or above the target value in the above table. Or, demonstration of maximum possible performance given any hardware coherence limitations.

**Deliverable 3:** GHZ state optimization through improved two-qubit waveform pulse protocols.

**Description:** Using the novel two-qubit gate waveforms, Q-CTRL will test the fidelity of GHZ state preparation and identify residual errors likely arising from circuit-level sources, such as crosstalk. Only gate-level improvements will be used during these experiments on the current 5 qubit devices.

Deliverable 4: Routine transfer to advanced devices

**Description:** All work from Deliverables 1, 2, and 3 will be ported over to the new advanced device types.

Success Criteria: N/A

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#### Part 2: Delivery: June 30, 2025

#### • Scale up to 5-qubit

Deliverable: Integration of new two-qubit gate subroutines.

Description: Upon completion of Part 1, Q-CTRL will provide an integrated version of those Part 1 routines for Sinica to use as needed. This includes native support for Quantum Machines controllers, and validation within their existing software infrastructure. This will only be done for the advanced devices.
Success Criteria: Fully integrated solutions that provide the ability to invoke the new two-qubit gate optimization routine within the Sinica environment.

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## Part 3: Delivery: December 1, 2025

### • Scale up to 20-qubit

Deliverable: Collaborating on next steps

Description: Based on the results and findings from Part 1 and 2, Q-CTRL will provide one or more options for continued performance improvements (unless none are evident). This may include:

- 1. Further GHZ state optimizations based on circuit-level error suppression
- 2. Automation and scope expansion of existing gate optimization protocols.
- 3. A report of additional findings from Phase 1 and 2 of performance limiting factors not related to Q-CTRL scope (for example hardware related limitations)

Success Criteria: Options delivered to Sinica and decisions made about next steps

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